Advanced coupled voltage-frequency control for power efficient DVFS management

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Abstract

Power management is a hot-topic in complex System-on-Chip (SoC) designs. In the context of advanced technologies, Dynamic Voltage-Frequency Scaling (DVFS) techniques are widely proposed to improve efficiency. Nowadays, these mechanisms are composed of independent actuators controlling the applied voltage and clock frequency. A predefined sequence has to be used to switch from one state to another in order to avoid timing faults but increasing the energy cost. The timing of the sequence depends on the dynamic response of actuators. In this work, an external controller is designed in order to couple both actuators to manage the voltage and frequency transient periods, increasing power efficiency. The proposed controller has been implemented to couple a Vdd-hopping mechanism with a Frequency-Lock Loop circuit.

Keywords : Dynamic voltage frequency scaling, control, power aware system, system stability.

1 Introduction

The growing demand for more autonomy of mobile equipments at the same time that general purpose microprocessors hitting the power wall, increases the necessity to research technique for rising power-efficiency of computing. Actually, power consumption is a limiting factor in Very-Large-Scale Integration (VLSI), especially for mobile applications. Dynamic Voltage and Frequency Scaling (DVFS) [9] has proven to be highly effective to reduce the power consumption of the chip while meeting the performance requirements [10]. The key idea behind local DVFS is to control the supply voltage and the frequency of a circuit at runtime to minimize the power consumption while satisfying the computation/throughput constraints [8]. The DVFS technique mainly rely on two actuators. These drivers need to be dynamically controlled in order to reduce the power consumption while maintaining the required performance. More precisely, the control policy must be carefully designed in order to achieve high power efficiency at low area cost. The voltage driver fixes the supply voltage of

the circuit. It can be a classical buck converter [11] or a Vdd-hopping converter [4, 12]. On the other side, the frequency actuator is a clock generator classically based on a Phase-Locked Loop (PLL) or a Frequency-Locked Loop (FLL).

On traditional synchronous CMOS circuits, the applied clock frequency should be chosen considering the supply voltage. For a given voltage a high frequency produces timing faults [13], i.e. the clock cycle provides not enough time for logic cells to drive the output signals. On the contrary, a low frequency for a given voltage will result on poor calculation performance for a high energy consumption. For these reasons, the actuators management policy should ensure a predefined sequence to change from one voltage-frequency state to another. For instance, for an increasing frequency step the management policy should firstly increase the supply voltage, and once the output is stabilized, the frequency can be increased. The timing of this sequence depends on the dynamic response of actuators.

A consequence of technology scaling in advanced CMOS technologies is the in-die and die-to-die process variability. From a practical viewpoint, it is becoming increasingly difficult to manufacture integrated circuits with tight parametric values [12]. In addition, circuit parameter are more sensible to temperature and voltage variations. Therefore, in order to obtain optimal performance, the clock frequency must be controlled according to Process, Voltage and Temperature (PVT) variations. Recently, control techniques have been applied to develop DVFS drivers. For instance, in [4, 7], the closed-loop control of the voltage actuator is dealt with; and in [5], a robust control for a Frequency Lock-Loop (FLL) is presented.

In these previous works, the internal control of every driver has been independently treated. However, in order to improve DVFS efficiency, every PVT variation should impact the sequence timing of the management of drivers. This work deals with a joint control of voltage and frequency drivers, increasing power efficiency and avoiding timing faults. The proposed joint control allows to manage devices with different dynamics, allowing to simultaneously apply voltage and frequency set-point steps and providing global stability.

The rest of this paper is organized as follows: in Section 2, the problem statement is established. Architecture and internal control of each actuator are presented in Section 3. Next, Section 4 is consecrated to the joint control technique. Some simulations are presented in Section 5. The paper ends with conclusions and future work.

Notation. For a given $x \in \mathbb{R}$,

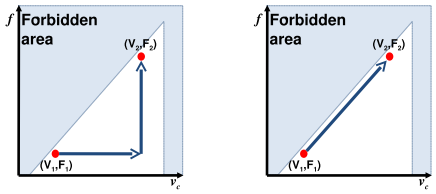
$$\mathrm{sat}_m^M(x) \triangleq \begin{cases} M & \text{if } x > M \\ x & \text{if } m \leq x \leq M \\ m & \text{if } x < m \end{cases}$$

$\Delta x \triangleq x_k - x_{k-1}$ is the value of x in two consecutive sampling time. Finally, $\mathcal{L}_2$ is the space of $\{x_k\}$ with the norm: $\|x_k\|_2^2 \triangleq \sum_{k=0}^{\infty} x_k^T x_k < \infty$, i.e., it is bounded energy.

2 Problem statement

DVFS circuitry applies voltage v_c and frequency f to the functional synchronous circuit. Depending on the integration technology, each possible supply voltage

allows a maximum clock frequency without timing faults. Moreover, a very high voltage produces permanent circuit damages. In the voltage-frequency plane and in the context of this work, these constraints are approximated by a forbidden area as shown in Fig. 1a. In order to improve efficiency, the DVFS mechanism changes the applied voltage and frequency values in a sequential way in order to avoid the circuit to get into the forbidden area. For instance, for changing from a set-point (V_1, F_1) to another one (V_2, F_2), where $V_1 < V_2$ and $F_1 < F_2$, firstly voltage is changed while frequency is remained constant, and latter frequency is changed while voltage is constant, and vice-versa [6].



(a) Without joint control.

(b) With joint control.

Figure 1: Evolution of v_c and f.

The problem statement considers to jointly control the voltage and frequency drivers in order to follow an optimal transition from (V_1, F_1) to (V_2, F_2) as represented in Fig. 1b, instead of using a sequential management as in Fig. 1a. This new strategy improves the system efficiency and matches the different dynamics of driver while guaranteeing global system stability.

3 Actuator architecture and control

As mentioned before, in this work the DVFS is implemented by Vdd-Hopping and FLL drivers. Each circuit is independently controlled by an internal control law. The very lengthy algebraic calculations required to derive the results presented here are omitted due to lack of space; they may be found in [4, 5].

3.1 FLL

The main blocks of the FLL are modeled through design considerations and accurate simulations. These blocks are a Digitally-Controlled Oscillator (DCO) that provides a clock, a sensor (i.e. a counter) to measure the clock frequency, a comparator that compares the output clock frequency with the target one, and a digital controller. In Fig. 2, a sketch of the FLL is shown.

Digitally-Controlled Oscillator. The DCO was firstly designed considering technological parameters for the delay cells. Then, based on accurate low-level simulations (Spice level), a linear DCO model has been approximated. It has been assumed that this model evolves over the time with PVT variations [5]. The simplified DCO model is:

$$f_k = b + K_{DCO} u_{fk} + B_w \nu_{f_k} \tag{1}$$

where $f, f_k \in \mathbb{R}^1$ are the analog and digital frequency output respectively, $u_{fk} \in \mathbb{N}$ is coded over 8 bits between 0 and 255 and it is a digital representation of a

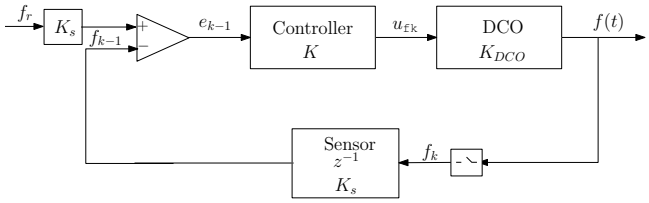


Figure 2: FLL architecture.

clock frequency. T_{sf} is the sampling period, b is the DC-offset, K_{DCO} is a gain. ν_f is a bounded energy signal to take into account any possible disturbance, and B_w is a constant that defines the disturbance magnitude. In order to take into account the PVT variation effects, it is assumed that parameters K_{DCO}, b and B_w can change in a certain interval.

Sensor. The digital sensor counts the number of generated clock peaks during a sampling period of time. This sensor introduces a delay of one sampling period that is represented in the feedback loop model:

$$M_k \triangleq K_s f_{k-1}$$

Control. Define $e_k \triangleq K_s(f_r - f_k)$, where f_r is the reference signal and K_s is a positive constant that represents the sensor gain. Then, the error equation is:

$$e_k = -b - K_{DCO} u_{fk} - B_w \nu_{f_k} + K_s f_r \tag{2}$$

In order to limit the FLL area cost and taking into account the control objectives, a simple digital integral controller is defined:

$$u_{fk} = u_{fk-1} + K(K_s f_r - M_k) = u_{k-1} + K_f e_{k-1} \tag{3}$$

where K_f is a controller parameter to be tuned ensuring:

- closed-loop stability;
- robustness against PVT variations;
- suited performance (no overshoot, no static error, short transient period);
- low area overhead and
- exogenous disturbance rejection.

In [5], a method for obtaining an optimal and robust H_∞ control has been presented, which accomplishes all requirements given above.

3.2 Vdd-Hopping

In [12] a discrete circuit that handles two-voltage levels with a Vdd-Hopping technique accomplishing a DVS architecture was presented in order to reduce power consumption. The Vdd-Hopping circuit is composed of: a high voltage supply, V_h; a low voltage supply, V_l; a set of PMOS transistors connected in parallel between V_h and the core voltage, v_c, and a PMOS transistor connecting V_l to v_c when the low voltage level is the steady-state. The set of parallel

PMOS transistors allows evolving the output voltage from a low voltage level to a high voltage level (rising transient period) and from a high voltage level to a low voltage level (falling transient period). The steady-state must correspond to a high voltage level or a low voltage level. For simplicity, the low voltage supply, V_l, as well as the PMOS transistor connecting it to v_c are disregarded for control design purposes. The main objective is to ensure that v_c achieves the two voltage levels by switching the PMOS transistors. Fig. 3 represents this circuit. In this architecture, at least, one transistor must always be switched on.

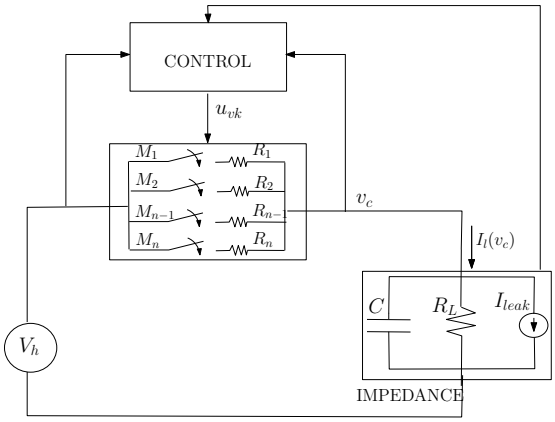


Figure 3: Vdd-hopping architecture.

The voltage loop equation yields to the relationship:

$$\frac{V_h - v_c}{R_{u_{vk}}} = \frac{v_c}{R_L} + I_{leak} + C\frac{dv_c}{dt} \tag{4}$$

where $R_{u_k} \triangleq \frac{R_0}{u_{vk}}$, u_k being the number of transistors switched on, thus, $u_{vk} \in \mathcal{U} = \{1, 2, ..N\}$ and it is the control variable.

The system load (fed circuit) is represented as an impedance which depends on the applied clock frequency f and on v_c [12]. It is composed of a current supply, I_{leak}, a capacitance, C, and a dynamic resistance, $R_L(f, v_c)$, representing the dynamic and short-circuit consumption. I_{leak} is assumed constant. In this work, the load model presented in [12] is employed.

Consider $\epsilon_k \triangleq v_r - v_{ck}$ where v_r is the voltage reference and v_{ck} is the sampling core voltage. Now, from Eq. (4), the approximated discrete-time voltage error equation is:

$$\epsilon_{k+1} = (1 - T_s\beta)\epsilon_k + T_{sv}b(v_r - V_h)u_{vk} + T_s(\beta v_r + \delta - bu_{vk}\epsilon_k) + \nu_{vk} \tag{5}$$

where ν_{vk} is an additional exogenous disturbance from v_r and it is $\mathcal{L}^2$, $\beta \triangleq \frac{1}{R_L C} > 0$, $\delta \triangleq \frac{I_{leak}}{C} > 0$ and $b \triangleq \frac{1}{R_0 C} > 0$. T_{sv} must be less or equal to the smaller $\frac{1}{f}$. The approximated time-discretization (5) is performed by using the forward Euler method, by assuming that the sampling time is small enough to the system evolution.

The proposed controller for this system is based on a linear controller [3]:

$$u_{v_k} = \text{sat}_1^N \left\{ u_{vk-1-h_1} + \text{round}\left(K_1 \Delta\epsilon_{k-h_1-h_2} + K_2 \epsilon_{k-h_1-h_2 1}\right) \right\} \tag{6}$$

where h_1 and h_2 are sampling-period delays and $h \triangleq h_1 + h_2$. K_1 and K_2 are controller parameters and they must be tuned in such a way that the following properties are ensured:

- closed-loop stability;
- robustness regarding PVT variations and delays;
- suited performance (no current peaks, no static error, short transient period);
- low area overhead and
- exogenous disturbance rejection.

In [4], a state-space representation was given by (5) and a mechanism has been presented in order to compute K_1 and K_2 for achieving optimal and robust control, which accomplish almost all requirements given above. Only, the rejection of exogenous disturbance was not considered. An easy extension of this method is performed here for taking into account this last requirement.

Theorem 2 presented in [4] is extended in order to consider any disturbance input. Assume, there exists a minimum disturbance attenuation, $\gamma^* \geq 0$, such that, for all $\gamma \geq \gamma^*$ the $\mathcal{L}_2$ gain between the disturbance vector ν_{v_k} and the output vector z_k is less or equal to γ. i.e.

$$\begin{aligned} &\|z_k\|_2^2 - \gamma^2 \|\nu_{v_k}\|_2^2 < 0, \quad \forall \nu_{v_k} \in \mathcal{L}_2 \\ &\text{for} \quad \phi_l = 0, \quad -h \leq l \leq 0. \end{aligned} \tag{7}$$

Assumption 1 *There exists a Lyapunov function V_k, with condition $V_{k+1} - V_k < 0$ and a γ, such that,*

$$V_{k+1} - V_k + z_{k+1}^T z_{k+1} - \gamma^2 (\nu_k^T \nu_k) \leq \zeta^T \Gamma \zeta < 0. \tag{8}$$

where $\zeta \triangleq [\epsilon_k \quad \epsilon_k - \epsilon_{k-1} \quad \psi_k \quad \nu_k]^T$ is an augmented state vector and $\Gamma \in \mathcal{R}^{4\times 4}$ is a symmetric matrix.

Theorem 1 *Consider system (5) and control law (6) with $h_1, h_2 \geq 0 \in \mathbb{N}$ known constant delays and $K, G \in \mathbb{R}^{1\times 2}$. If there exist $T, Y, B \in \mathbb{R}^{2\times 1}$ and $Q_1 \in \mathbb{R}^2$ with $K_v = TQ_1^{-1}$, $G = YQ_1^{-1}$, $A, \mathcal{Q}, \mathcal{R}, \bar{R}, \bar{P}_1, \bar{S} > 0 \in \mathbb{R}^2$ for $j = 1, ..., 64$ and $c, \mu, \gamma > 0$ such that:*

$$\begin{aligned} min_K \quad & \mu \\ & \bar{P}_1 > 0 && (9) \\ & \bar{\Gamma}^{(j)} < 0 \quad j = 1, ..., 64, && (10) \\ & \begin{bmatrix} \bar{P}_1 - \mu & 0 & 0 \\ * & \bar{S} - \mu & 0 \\ * & * & \bar{R} - \mu \end{bmatrix} < 0, && (11) \\ & \Lambda > 0 && (12) \end{aligned}$$

being $\bar{\Gamma}^{(j)}$ defined in Eq. (13), found at the top of next page, are satisfied. Then, in the vertices j, the equilibrium is asymptotically stable as well as the current peaks are limited in the entire polytope.

$$\bar{\Gamma}^{(j)} \triangleq \begin{bmatrix} \bar{\Gamma}_1^{(j)} & \bar{\Gamma}_2^{(j)} & -\bar{\Xi}^{(j)^T} + \bar{S} & Q_1 & \bar{\Xi}^{(j)} & \bar{\Xi}^{(j)} & Q_1 \\ * & \bar{P}_1 - 2Q_1 + h\bar{R} & 0 & 0 & 0 & 0 & Q_1 \\ * & * & -\bar{R} - \bar{S} & 0 & 0 & 0 & 0 \\ * & * & * & -\mathcal{Q}^{-1} & 0 & 0 & 0 \\ * & * & * & * & -\mathcal{R}^{-1} & 0 & 0 \\ * & * & * & * & * & -\mathcal{R}^{-1} & 0 \\ * & * & * & * & * & * & -\gamma^2 I \end{bmatrix}, \tag{13}$$

where

$$\bar{\Xi}^{(j)} \triangleq (\alpha_k^{(j)} T + (1 - \alpha_k^{(j)}) Y), \quad \bar{\Gamma}_1^{(j)} \triangleq Q_1 {A^{(j)}}^T + A^{(j)} Q_1 - 2Q_1 + \bar{\Xi}^{(j)^T} + \bar{\Xi}^{(j)},$$
$$\bar{\Gamma}_2^{(j)} \triangleq \bar{P}_1 + Q_1 {A^{(j)}}^T - 2Q_1 + \bar{\Xi}^{(j)^T}$$

Proof 1 *The proof is an extension of the proof presented in [4] for Theorem 2, taking into account the functional cost* (7)*.*

The implementation of the controller described of equation (6) requires a low area overhead. The saturation function is due to the control signal constraint mentioned before. The control objective is to achieve a reference signal. An control structure for the Vdd-Hopping circuit that manages current peaks is patent pending [1].

4 Joint control

As explained before, the main deal in this work is to jointly control the evolution of the frequency output of the FLL and the evolution of the voltage output of the Vdd-Hopping in order to reduce the power consumption. The solution presented here is shown in Fig. 4.

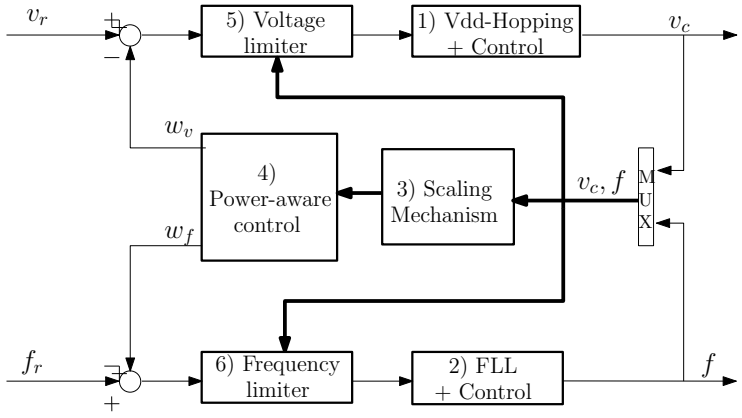


Figure 4: DVFS system with joint control.

This mechanism is composed of:

1. **Voltage actuator.** This circuit is a stable Vdd-Hopping circuit, Eq. (4), with its internal control law, Eq. (6), and a sampling time T_{vs}.

2. **Frequency actuator.** In this block, there is a stable FLL, Eq. (1), with its internal control law, Eq. (3), and a sampling time T_{fs}.

3. **Scaling mechanism.** This mechanism allows to compensate the different dynamics of the two actuators. Note that each actuator presents a different sampling period. In this block the faster dynamic is *under-sampled*.

4. **Power-aware control.** It generates perturbations that are added to the corresponding references, in such a way that both references evolve following a given trajectory that induces an increase of power efficiency.

5. **Voltage limiter.** This block ensures that the system voltage will not reach the forbidden area.

6. **Frequency limiter.** This block, similar to block 5), ensures that the applied frequency will not reach the forbidden area.

4.1 Joint control

The joint power-aware control (block 4) is defined as:

$$\begin{bmatrix} w_v \\ w_f \end{bmatrix} \triangleq \begin{bmatrix} v_{c_k} - \frac{f_k - F_0}{M} \\ f_k - (F_0 + M v_{c_k}) \end{bmatrix} = \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} \epsilon_k \\ \frac{e_k}{K_s}, \end{bmatrix}$$

where F_0 and M are parameters that define the optimal trajectory of the variable states in order to improve power efficiency. This optimal path is defined by $f_k = F_0 + M v_{c_k}$. Remind $e_k = K_s(f_r - f_k)$ and $\epsilon_k = v_r - v_{ck}$. Let rewrite in a compact way:

$$w_k = -L x_k \tag{14}$$

where $w_k \triangleq [w_{vk} \quad w_{fk}]^T$, $x_k \triangleq [\frac{e_k}{K_s} \quad \epsilon_k]^T$, $L \in \mathbb{R}^{2\times 2}$ is semidefinite positive matrix, thus, it is not inversible. w_k is added to the reference, as shown in Fig. 4.

Remark 1 *L is a connection matrix, whose terms define the optimal trajectory that the state must follow in order to achieve the consensus.*

Assumption 2 *Consider a closed loop system under the form*

$$\vec{x}_{k+1} = (\mathcal{A} + \mathcal{B}\vec{K})\vec{x}_k, \tag{15}$$

with $\vec{x}_k = [\frac{e_k}{K_s} \quad \epsilon_k \quad \epsilon_{k-1}]^T \in \mathbb{R}^{1\times 3}$ and $\mathcal{A}+\mathcal{B}\vec{K} = diag\{a+b\vec{K}_f, \quad A+B\vec{K}_v\} \in \mathbb{R}^{3\times 3}$ where $a+b\vec{K}_f$ is a FLL closed loop and $A+B\vec{K}_v$ is a Vdd-Hopping closed loop. This system is stable and robust as well as it does not present overshoots.

Theorem 2 *There exists a system* (15)*, whose input is perturbed by* (14)*. Consider a definite positive matrix $\mathcal{P} \in \mathbb{R}^{3\times 3}$ associated to the stability of system* (15)*, such that,*

$$\begin{bmatrix} -(\bar{L}+\mathcal{P}) & (\mathcal{A}^T + \vec{K}^T\mathcal{B}^T - \bar{L}^T\vec{K}^T\mathcal{B}^T)(\bar{L}+\mathcal{P}) \\ * & -(\bar{L}+\mathcal{P}) \end{bmatrix} < 0 \tag{16}$$

where $\bar{L} \in \mathbb{R}^{3\times 3}$ is an augmented vector from $L \in \mathbb{R}^{2\times 2}$, in order to be agree with the dimension of $\vec{x}_k$. Then, Lx_k converges to zero and the system is globally asymptotically stable.

Proof 2 *The global system is*

$$\vec{x}_{k+1} = (\mathcal{A} + \mathcal{B}\vec{K} - \mathcal{B}\vec{K}\bar{L})\vec{x}_k. \tag{17}$$

Take as Lyapunov function:

$$U_k = \vec{x}_k^T \bar{L}\vec{x}_k + \vec{x}_k^T \mathcal{P}\vec{x}_k \geq 0,$$

in order to make that $\bar{L}\vec{x}_k$ converges to zero at the same time that $\vec{x}_k$ converges to zero. Note that $\bar{L}$ is semidefinite positive.

$$\begin{aligned} U_{k+1} - U_k &= (\vec{x}_{k+1}^T(\bar{L} + \mathcal{P})\vec{x}_{k+1} - \vec{x}_k^T(\bar{L} + \mathcal{P})\vec{x}_k) \\ &= \vec{x}_k^T \Big[\mathcal{A}^T + (I_3 - \bar{L}^T)\vec{K}^T\mathcal{B}^T)(\bar{L} + \mathcal{P}) \\ &\quad (\mathcal{A} + \mathcal{B}\vec{K}(I_3 - \bar{L}) - (\bar{L} + \mathcal{P})\Big] \vec{x}_k < 0 \end{aligned}$$

Applying Schur complement and pre- and post- multiplying matrix by $[I_3 \quad (\bar{L} + \mathcal{P})]$ LMI (16) is achieved.

Remark 2 *The global system composed of:*

- *discrete models of the FLL (1) and Vdd-Hopping circuit (4), with their corresponding controllers (3), (6), that, among others, reject disturbance and*
- *the joint control mechanism*

is globally asymptotically stable from Theorem 2.

4.2 Voltage and frequency limiter

The voltage and frequency references with their corresponding perturbations are saturated in the limiter blocks 5) and 6) as follows:

$$sat^{V_h}_{\frac{f-F_0}{M}}(v_r + w_{vk}) \tag{18}$$

$$sat^{F_0+Mv_c}_{f_{min}}(f_r + w_{fk}) \tag{19}$$

Remark 3 *The internal control of the FLL (3) ensures that there is no overshoot. Likewise, the Vdd-hopping is an approximate first-order system (see Property 1 in [2]). Consequently, there is no overshoot in the voltage and frequency outputs.*

Corollary 1 *From limiters (18)–(19) and Remark 3 timing faults are avoided, i.e., the state does not go to the forbidden area.*

5 Simulations

The proposed joint control has been evaluated in the Matlab environment. For this test-case, the FLL are reported from [5]. The sampling period is $60ns$ and the control gain is $K = 0.392$. Likewise, for the Vdd-Hopping system is taken from [4] with a sampling period of $2ns$. The control gains are $K_1 = -1.24$, $K_2 = 0.22$. $(V_1, F_1) = (0.8V, 50LSB)$ and $(V_2, F_2) = (1.11V, 200LSB)$. For the joint control $M = 485$ and $F_0 = -335$.

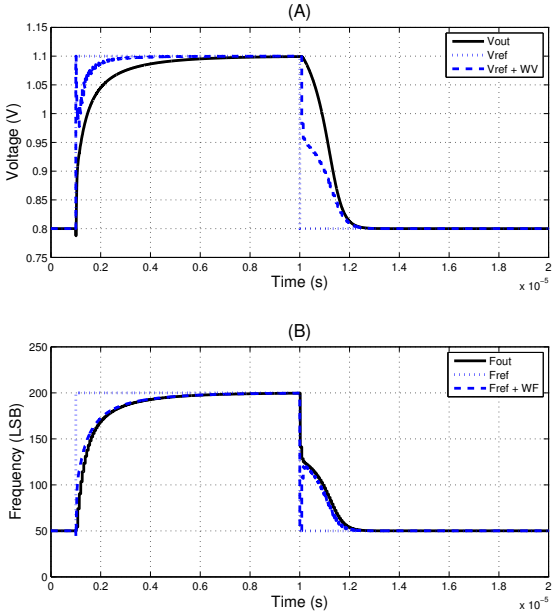


Figure 5: Evolution of voltage-frequency with joint control.

Figure 5 shows the evolution of both voltage and frequency when the joint control is implemented for rising and falling steps. For the same scenario, Fig. 6 shows the w_v and w_f evolution when system is rising from (V_1, F_1) to (V_2, F_2) and dropping from (V_2, F_2) to (V_1, F_1). The changing commands have been applied at $2\mu s$ for the rising step and at $10\mu s$ for the dropping step. Note that the rising and dropping evolutions are not symmetrical due to the limiters (Eq. (18)–(19)) that avoid timing faults and the non-linear nature of voltage driver. In Fig. 7 the voltage-frequency evolution in the VF plane is shown. Note that, as indeed, the DVFS circuit does not cross the reference trajectory, which also limits the forbidden area.

Finally, the power consumption has been analyzed for a rising step, comparing the joint control with an equivalent non-coupled system. A safe sequence has been established for the non-coupled system, applying firstly a rising voltage step at $2\mu s$ and then a rising frequency step at $5\mu s$. Total transition period corresponding to the trajectory from (V_2, F_2) to (V_1, F_1) represented in Fig. 1a, is estimated to $7\mu s$. Figure 8 shows the normalized power comparison for this period. The energy gain for this interval has been estimated to 40.5%.

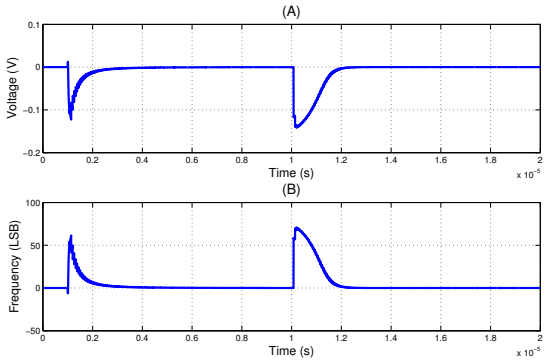


Figure 6: Evolution of voltage and frequency perturbations.

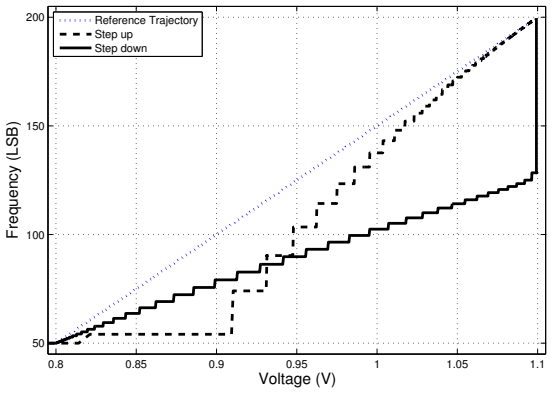


Figure 7: Evolution of voltage and frequency.

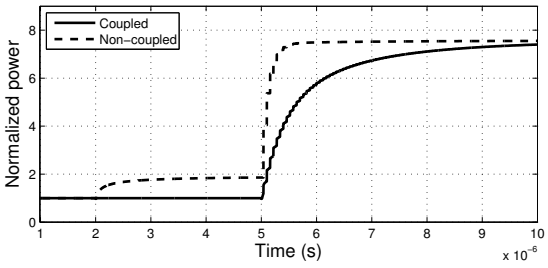


Figure 8: Power comparison for coupled and non-coupled systems.

6 Conclusions

In this work, a joint controller has been designed to jointly manage voltage and clock frequency in DVFS mechanism. It has been implemented to control a Vdd-Hopping driver and a FLL clock generator. The internal controller of each driver was studied in [4, 5]. Among other characteristics, these independent closed-loop systems reject perturbations and provide outputs without signal overshoots. From these properties, it has been designed an external joint controller, in such a way that the complete system is globally stable. Finally, a limiter was introduced in each reference in order to guarantee that there is no timing faults. This joint controller has been validated through Matlab simulations. It has been shown, that the power consumption can be reduced by 40.5% in the evaluated test-case. As future work, a attraction region induced by limiters (18)–(19) will be estimated. Likewise, it is expected to validate these results in Spice.

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